PATENT CLAIMS

1. Circuit for producing said galvanically separated synchronization impulses (sync) from an AC mains,

characterized in that

the line voltage rectified by means of a said half-wave rectifier (D1), lies on a said voltage divider (R1, R2) for the switching input of a said semiconductor switch (T1), and the said emitting diode of a said optocoupler (OKO) lies in the working branch, whereby the working branch has, in series with the said emitting diode (DO) a said drop resistor (R3), via which a said storage capacitor (C2) can be periodically charged and can be discharged via the said emitting diode (DO), and at least one said transistor (T2, T3) is arranged downstream of the said receiving element (EO) of the said optocoupler (OKO), which is fed by a said voltage source (Ub) that is galvanically separated from the line voltage and in whose load branch the essentially rectangular synchronization impulses (sync) are available.

2. Circuit in accordance with claim 1, characterized in that the semiconductor switch is a said transistor (T1).

3. Circuit in accordance with claim 1 or 2, characterized in that a said voltage-limiting Zener diode (D2) lies parallel to the said storage capacitor (C2).

4. Circuit in accordance with one of the claims 1 through 3, characterized in that the series connection of the said drop resistor (R3), the said emitting diode (DO) and a said current-limiting resistor (R4) lies in the working branch of the said switch (T1), whereby the said storage capacitor (C2) lies parallel to the emitting diode-current-limiting resistor-switching junction series connection.

5. Circuit in accordance with claim 4, characterized in that a said resistor (R5) lies parallel to the said emitting diode (DO) for defining the potential.

6. Circuit in accordance with one of the claims 1 through 5, characterized in that a said filter capacitor (C1) lies parallel to a said resistor (R2) of the input voltage divider, which lies parallel to the base emitter junction of the said input transistor (T1).

7. Circuit in accordance with one of the claims 1 through 6, characterized in that the said transistor (T2) arranged downstream of the said receiving element (EO) is a Darlington transistor.

8. Circuit in accordance with one of the claims 1 through 7, characterized in that another said transistor (T3) for phase reversal is arranged downstream of the said transistor (T2), which is arranged downstream of the said receiving element (EO) of the said optocoupler (OKO), whereby the synchronization impulses are available at the said working resistor (R8).